What is claimed is:

1. A timing data register array for sensing and storing data outputted through a data bus in a multi-bit line structure cell array for inducing a sensing voltage of a main bit line by converting a sensing voltage of a sub bit line into current, the timing data register array comprising:

a bus pull-up unit for pulling up the data bus in precharge;

a sense amp unit for sensing a sensing voltage of the data bus according to a preset sensing threshold voltage; and

a timing data sensing unit for sensing a sensing value of the sense amp unit by using timing of the sensing voltage of the pulled-up data bus to reach the sensing threshold voltage, and for outputting the sensing value to a data buffer.

2. The array of claim 1, wherein the timing data sensing unit comprises:

a lock switch unit for selectively transmitting the sensing value of the sense amp unit according to lock signals activated in different timings;

a data latch unit for storing the data transmitted

through the lock switch unit;

a data-out control unit for outputting the data stored in the data latch unit; and

a write switch unit for transmitting the data of the data-out control unit to the data bus to be restored in the cell array.

3. The array of claim 2, wherein the lock signals are previously measured according to the sensing threshold voltage and decrease of the sensing voltage of the data bus, and activated in the preset timings.

4. A ferroelectric random access memory including a multi-bit line structure cell array for inducing a sensing voltage of a main bit line by converting a sensing voltage of a sub bit line into current, the ferroelectric random access memory having a timing reference sensing function, comprising:

a plurality of cell array blocks having the cell arrays;

a common data bus shared by the plurality of cell array blocks, for transmitting read data and write data for the cell array blocks; and

a timing data register array unit connected to the common data bus, for sensing the read data and outputting

the write data to the common data bus,

wherein the timing data register array unit senses the read data by using timing of a sensing voltage of the common data bus to reach a sensing threshold voltage.

5. The memory of claim 4, wherein the timing data register array unit comprises:

a bus pull-up unit for pulling up the common data bus in precharge;

a sense amp unit for sensing the data of the common data bus according to the sensing threshold voltage, when receiving a sensing control signal;

a data latch unit for storing the read data and the write data;

a lock switch unit for selectively transmitting the output data from the sense amp unit to the data latch unit according to lock signals;

a data-in control unit for receiving the write data and transmitting the write data to the data latch unit in the write operation;

a data-out control unit for controlling output of the data stored in the data latch unit according to an operation mode; and

a write switch unit for transmitting a data of the data-out control unit to the common data bus to be restored

in the cell array blocks.

6. The memory of claim 5, wherein the lock signals are previously measured according to the sensing threshold voltage and decrease of the sensing voltage of the common data bus, and activated in the preset timings.

7. The memory of claim 6, wherein the lock switch unit comprises a transmission gate selectively turned on/off according to the lock signals, for selectively transmitting the data of the sense amp unit.

8. The memory of claim 5, wherein the data-out control unit outputs the data stored in the data latch unit to a data buffer and the write switch unit in the read mode, and to the data-out control unit outputs the data stored in the data latch unit to the write switch unit in the write mode.

9. The memory of claim 5, wherein the data-in control unit transmits the write data to the data latch unit when a column select signal is activated.

10. A data sensing method of a memory including a plurality of cell array blocks having a multi-bit line structure for inducing a sensing voltage of a main bit line

by converting a sensing voltage of a sub bit line into current, and a common data bus shared by the plurality of cell array blocks, the data sensing method using timing reference which senses data values of the common data bus by using different timings of sensing voltages of the common data bus corresponding to different data values to reach a sensing threshold voltage, respectively.

11. A data sensing method of a memory including a plurality of cell array blocks having a multi-bit line structure for inducing a sensing voltage of a main bit line by converting a sensing voltage of a sub bit line into current, and a common data bus shared by the plurality of cell array blocks, the data sensing method using timing reference, comprising:

a first step for calculating first timing and second timing of sensing voltages of the common data bus to reach a sensing threshold voltage by the sensing voltage of the sub bit line;

a second step for sensing the sensing voltages of the common data bus; and

a third step for storing and outputting the values sensed between the first timing and the second timing.

12. The method of claim 11, wherein the third step

activates lock signals between the first timing and the second timing, and senses and stores the sensing voltages at the time of activating the lock signals.

13. The method of claim 11, wherein the first and second timings are timings of the sensing voltages of the common data bus corresponding to data high and data low to reach the sensing threshold voltage.